Silicon High-Order Mode (De)Multiplexer on Single Polarization

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***Abstract*—Mode-division multiplexing on an integrated photonic chip is critical for future optical networks. High-order mode multiplexing is desired to increase the transmission capacity. Here, we propose and experimentally demonstrate a silicon on-chip high-order mode (de)multiplexer using subwavelength grating (SWG) structure, which supports 11-mode (de)multiplexing on a TE-polarized light (TE_0–TE_{10}). The proposed mode (de)multiplexer comprises three directional couplers and seven SWG-based directional couplers. Measurement results show that all the 11 channels have low crosstalk values (−15.4 to −26.4 dB) and low insertion losses (0.1 to 2.6 dB) at 1545 nm. To the best of our knowledge, our device achieves the highest-order-mode (de)multiplexing on a silicon photonic chip.**

***Index Terms*—Mode, multiplexing, photonic integrated circuits, silicon photonics, subwavelength grating.**

I. Introduction

ON-CHIP mode-division multiplexing (MDM) leverages the spatial modes of multimode waveguides, and allows significant scaling of transmission capacity for optical communication and interconnect systems [1]–[4]. Low-loss and low-crosstalk mode (de)multiplexers are important components in integrated silicon MDM systems. Various types of mode (de)multiplexers have been reported based on multimode interference (MMI) couplers [5]–[7], asymmetric Y-junctions [8]–[11], asymmetric directional couplers (DCs) [12]–[15], grating assisted couplers [16], [17], densely packed multimode waveguide arrays [18], [19], tapered directional couplers [20], [21], and Bragg grating and strip waveguides [22], [23]. Among them, asymmetric DC-based mode (de)multiplexers have attracted much attention benefitting from their compact footprints and scalabilities. Eight-channel mode (de)multiplexers on 2 polarizations ($TE_0 \sim TE_3$, $TM_0 \sim TM_3$) were proposed and demonstrated based on cascaded asymmetric DCs [14], [15]. Recently, D. Dai *et al.* proposed a scheme by employing dual-core adiabatic tapers to realize 10-channel mode (de)multiplexing on 2 polarizations ($TE_0 \sim TE_5$ and $TM_0 \sim TM_3$ modes) [21]. To the best of our knowledge, the highest-order mode multiplexing on the silicon-on-insulator (SOI) platform was TE_5 mode [21]. Robust higher-order mode (de)multiplexing is highly desired to further increase the communication capacity.

It is challenging to implement higher-order mode multiplexing using conventional DCs, due to the fact that the TE_0 mode in an access waveguide and the high-order mode in a bus waveguide have significantly different dependences of the effective refractive indices on the waveguide widths. If the dimensions of the waveguides change owing to fabrication errors, the coupling condition can be easily lost. To solve this problem, we propose an effective scheme to relax the mode multiplexer's tolerance to waveguide width variations. The idea is to design the access waveguide with a lower material index than that of the bus waveguide, therefore the two waveguides can have similar dependences of the mode effective indices on the waveguide widths. If the waveguide dimensions fluctuate, the effective indices of the two waveguides change equally, and the phase matching condition is still maintained. This can be realized by replacing the silicon access waveguide with a different refractive index material (e.g., silicon nitride), or more conveniently by using a subwavelength grating (SWG) structure without introducing other materials than silicon.

SWG is a periodic structure functioning as a homogenous medium [24]. The equivalent material refractive index n_{eq} of the SWG waveguide can be engineered by choosing an appropriate duty ratio of the grating. SWG has been used as fiber-chip couplers [25], waveguide crossings [26], MMI couplers [27], and fabrication-tolerant polarization splitter and rotators [28], [29]. By manipulating n_{eq} of the SWG waveguide, it is possible to engineer the dimensional dependences of the guided-mode effective indices on the waveguide width. This freedom in waveguide design enables robust high-order mode multiplexing by using SWG-based DCs. Previously we experimentally demonstrated a SWG-based 3-channel mode (de)multiplexer [30]. Fabrication-tolerant two-mode multiplexing utilizing two SWGs was also numerically studied [31]. Very-high-order mode (de)multiplexer can be designed and implemented with tolerance to waveguide width variations by using the SWG structure.

In this paper, we propose an on-chip mode (de)multiplexer using cascaded SWG-based DCs, and demonstrate 11-mode

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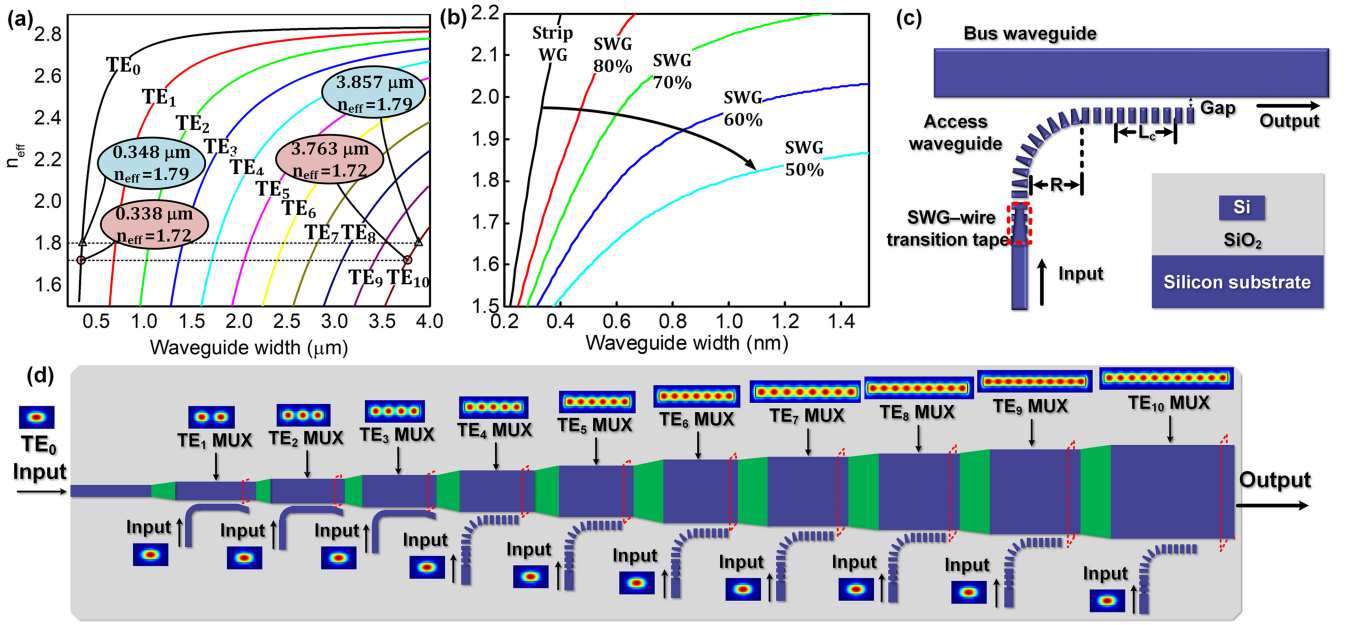

Fig. 1. Calculated effective indices of (a) eleven eigen-modes of the strip waveguides, (b) Bloch modes of the SWG waveguides with different duty cycles, as a function of the waveguide widths; (c) Schematic structure of a SWG-based DC, the inset shows the cross section of a silicon nanowire waveguide; (d) The schematic configuration of the proposed 11-mode multiplexer.

(de)multiplexing on a single polarized light ($TE_0 \sim TE_{10}$). Experimental results show reasonable insertion losses (<2.6 dB) and crosstalk values (<−15.4 dB) for all the 11 channels. To the best of our knowledge, it is the highest-order mode multiplexing on a silicon photonic chip. We also investigate the device's fabrication tolerance to waveguide width variations. If the waveguide widths vary by ±20 nm, our mode (de)multiplexer design shows acceptable insertion loss (<4.0 dB) and crosstalk value (<−10.4 dB) at 1545 nm. These results can be further optimized by modifying structural parameters.

II. Device Structure and Operation Principle

A. Challenges of Realizing High-Order MDM

Figure 1(a) shows the effective refractive index n_{eff} of the $TE_0 \sim TE_{10}$ modes as the waveguide width varies. The fundamental TE_0 mode and the higher-order modes have significantly different dependences of n_{eff} on the waveguide width. For instance, considering the coupling of a conventional DC, when the widths of the access and the bus waveguides are 0.338 μm and 3.763 μm, respectively, the phase-matching condition is satisfied between the TE_0 mode in the access waveguide and the TE_{10} mode in the bus waveguide. However, if the width of the access waveguide varies by 10 nm due to fabrication deviations, the width of the bus waveguide needs to change 94 nm to maintain the phase-matching condition, as shown in Fig. 1(a). Therefore, the coupling for the TE_{10} mode multiplexing can be easily lost. This is the main reason why the high-order mode (de)multiplexing is challenging to achieve by using conventional asymmetric DCs.

The solution we propose in this paper is to utilize the SWG structure. The equivalent material refractive index of the SWG structure is given by [32]:

$$n_{eq}^2 = \delta \cdot n_{Si}^2 + (1-\delta) \cdot n_{Clad}^2 \tag{1}$$

where n_{eq}, n_{Si}, and n_{clad} are the refractive indices of the equivalent material, silicon and cladding, respectively. δ is the duty cycle of the SWG structure. We calculate the effective indices of the SWG waveguides with different δ values as a function of the waveguide width, as shown in Fig. 1(b). By modifying the width and δ of the SWG waveguide, it is viable to engineer n_{eff} of the guided mode as well as the dependence of n_{eff} on the waveguide width.

B. Device Configuration and Simulated Results

Fig. 1(c) shows the schematic of the SWG-based DC. It consists of a strip bus waveguide and a SWG access waveguide. A SWG–wire transition taper [26] is used to couple the Bloch–Floquet mode in the SWG waveguide and the TE_0 mode in the silicon nanowire. The inset shows the cross section of a silicon nanowire waveguide. The thickness of the top silicon layer is 220 nm. To achieve highly-efficient mode coupling, the phase matching between the waveguides should be satisfied, i.e., the effective index of the TE_0 mode in the SWG access waveguide should be equal to that of the high-order mode in the bus waveguide. In this case, if a TE_0 signal is launched into the SWG waveguide, a high efficiency high-order mode signal can be obtained at the output port of the bus waveguide. The schematic configuration of the proposed on-chip silicon 11-mode (de)multiplexer ($TE_0 \sim TE_{10}$) is shown in Fig. 1(d). We employ three asymmetric DCs and seven SWG-based DCs to selectively couple the injected TE_0 modes to different high-order modes in a multimode bus waveguide.

TABLE I
PARAMETERS OF THE DESIGNED SWG-BASED DCS

Mode order	W_{access} (μm)	W_{bus} (μm)	δ	Gap (nm)	Coupling length (μm)	Taper length (μm)
TE_0	-	0.45	-	-	-	-
TE_1	0.439	0.875	-	190	18.5	16.5
TE_2	0.434	1.355	-	190	23.0	16.8
TE_3	0.405	1.705	-	190	20.0	12.9
TE_4	0.536	1.664	68%	140	4.5	1.4
TE_5	0.530	1.920	63%	100	2.6	9.7
TE_6	0.557	2.256	60%	100	12.7	12.2
TE_7	0.563	2.623	55%	200	6.0	14.0
TE_8	0.586	2.941	53%	200	6.0	10.7
TE_9	0.530	3.118	50%	200	4.0	6.4
TE_{10}	0.667	3.540	45%	200	5.0	15.0

The design process is described as follow: firstly, we calculate n_{eff} of the eigen-mode in the strip waveguide and the Bloch mode in the SWG waveguide as a function of the waveguide width, shown in Figs. 1(a) and 1(b). Then we compare the n_{eff} slopes of the eigen-mode and Bloch mode and choose a SWG waveguide with a specific δ for each mode coupling. Therefore, the Bloch mode in the access SWG waveguide and the high-order mode in the bus waveguide have the same dependences of n_{eff} on the waveguide width to achieve robust high-order mode multiplexing. Owing to the high dependence of n_{eff} on the waveguide width for TE_1, TE_2, and TE_3 modes as shown in Fig. 1(a), SWGs with large duty cycle values (>80%) are needed to realize robust phase matching for these three low-order modes, leading to a small feature size (<60 nm) in the fabrication. Hence, we utilize the conventional asymmetric DCs to replace the SWG-based DCs for these three modes to increase the feature size and to relax the fabrication requirement. Seven SWG-based DCs with different δ values are employed to multiplex $TE_4 \sim TE_{10}$ modes.

There are two requirements in designing the access waveguide width (W_{access}) and bus waveguide width (W_{bus}) for each mode: to satisfy the phase matching condition, and be tolerant to the waveguide width variations. Then the gaps between the two waveguides and their coupling lengths are optimized by iterative simulations via 3D finite-difference time-domain (3D-FDTD) method. Adiabatic tapers with a ~0.8° angle are used to smoothly connect the bus waveguides of different SWG-based DCs. Structural parameters including the dimensions of the waveguides, δ values of the SWG waveguides, gaps, coupling lengths and taper lengths are detailed in Table I. The periods of the SWG waveguides are chosen to be 300 nm to reach the sub-wavelength regime [24]. The width of the initial bus waveguide is chosen to be 0.45 μm to satisfy the single mode operation [34] and to maintain a low transmission loss. The bus waveguide and the SWG access waveguides are sufficiently separated using SWG waveguide bends, the curvature radii of the SWG waveguide bends are 10 μm and trapezoidal segments are adopted to reduce the bend loss [33]. It should be noted that some gap values are relatively small (e.g., 100 nm). Larger gaps can be chosen to relax the fabrication process, at the cost of longer coupling lengths.

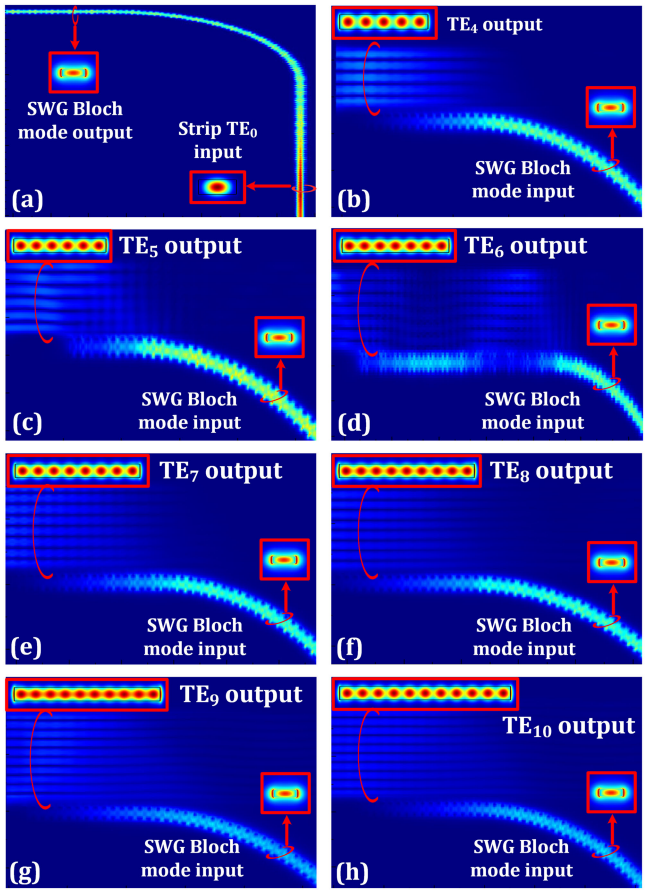

Fig. 2. (a) Light propagation along a SWG-wire transmission taper and a SWG waveguide bend; Simulated power distributions of the SWG-based DCs for the (b) TE_4, (c) TE_5, (d) TE_6, (e) TE_7, (f) TE_8, (g) TE_9, (h) TE_{10} modes, respectively.

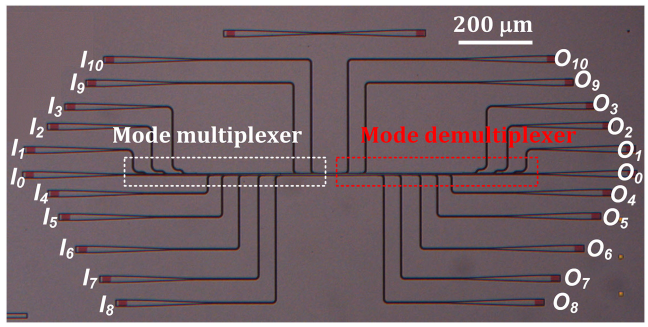

Fig. 3. Microscope photo of a fabricated mode (de)multiplexer device.

The mode conversion between a silicon nanowire waveguide and a SWG waveguide is shown in Fig. 2(a), simulated by 3D-FDTD method. The TE_0 mode in a silicon nanowire is coupled to the Bloch–Floquet mode by the transition taper and then transmitted through the SWG waveguide bend. The simulated power distributions of the proposed SWG-based DCs for the $TE_4 \sim TE_{10}$ modes are illustrated in Figs. 2(b-h), respectively. The insets show the mode distributions at the input and the output ports. When the Bloch modes are launched into the input ports of the SWG access waveguides, corresponding high-order modes can be obtained at the output ports of the bus waveguides.

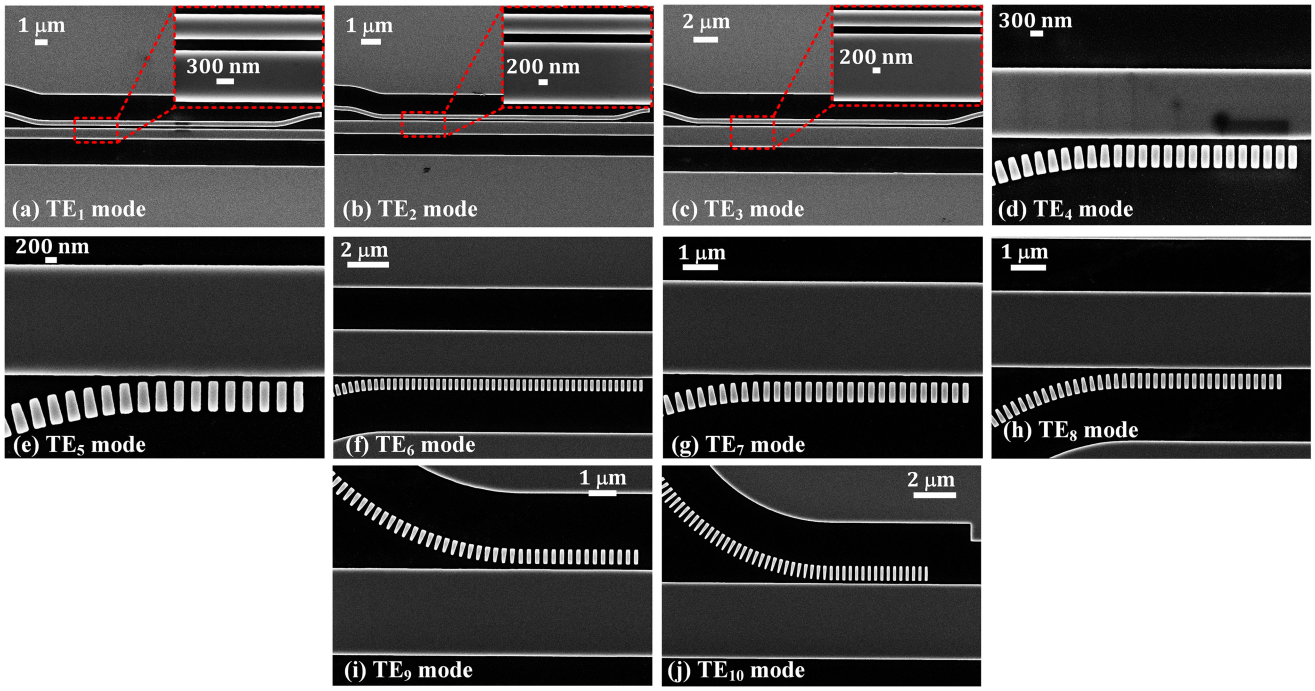

Fig. 4. Scanning electron microscope (SEM) images of the asymmetric DCs and the SWG-based DCs used for different-order modes. (a)–(j) depict the DCs for TE_1–TE_{10} mode coupling, respectively.

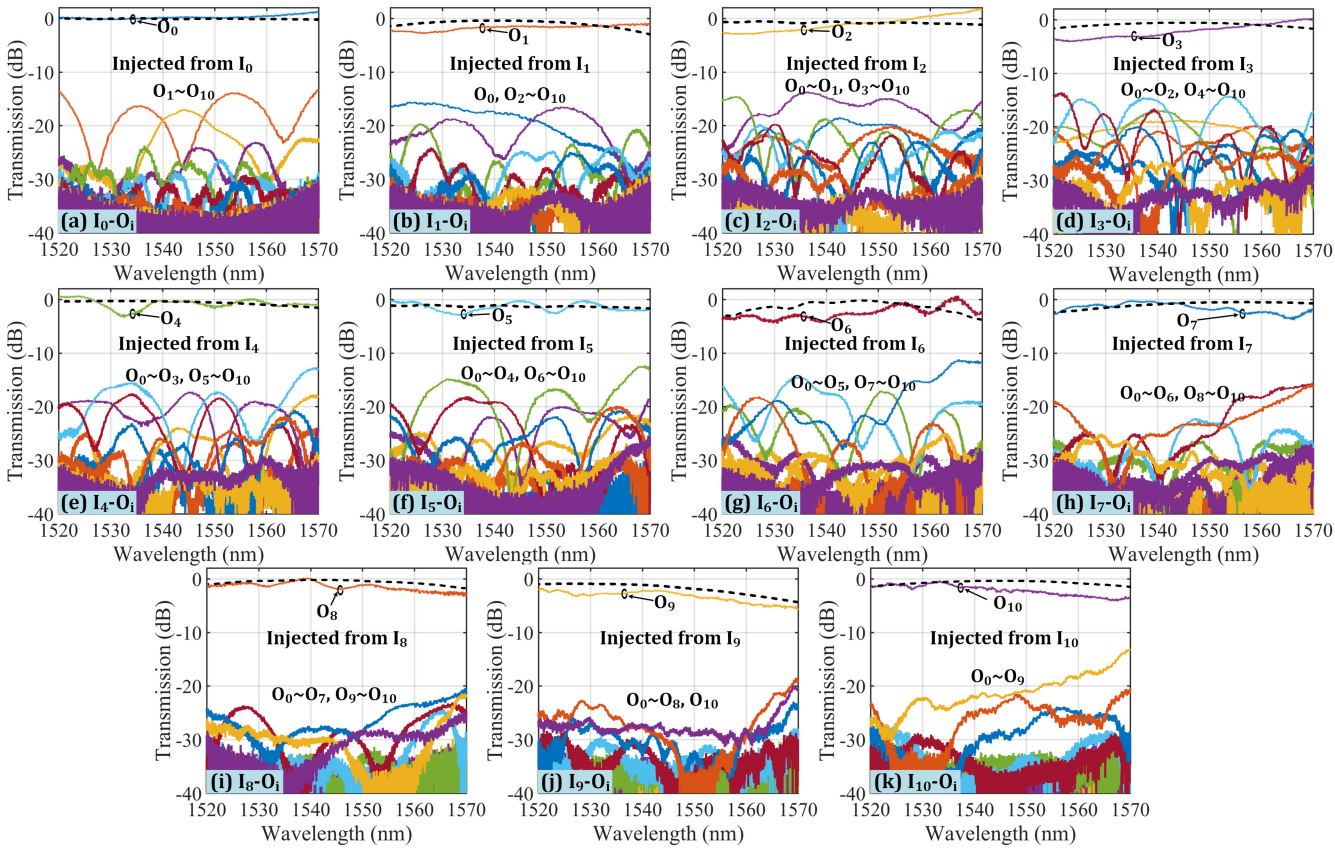

Fig. 5. (a)–(k) illustrate the measured transmission responses at the 11 output ports of the mode demultiplexer (denoted as O_i, $i = 0 \sim 10$), when the light is injected from different input ports I_0–I_{10}, respectively. The black dashed curves are the simulated results.

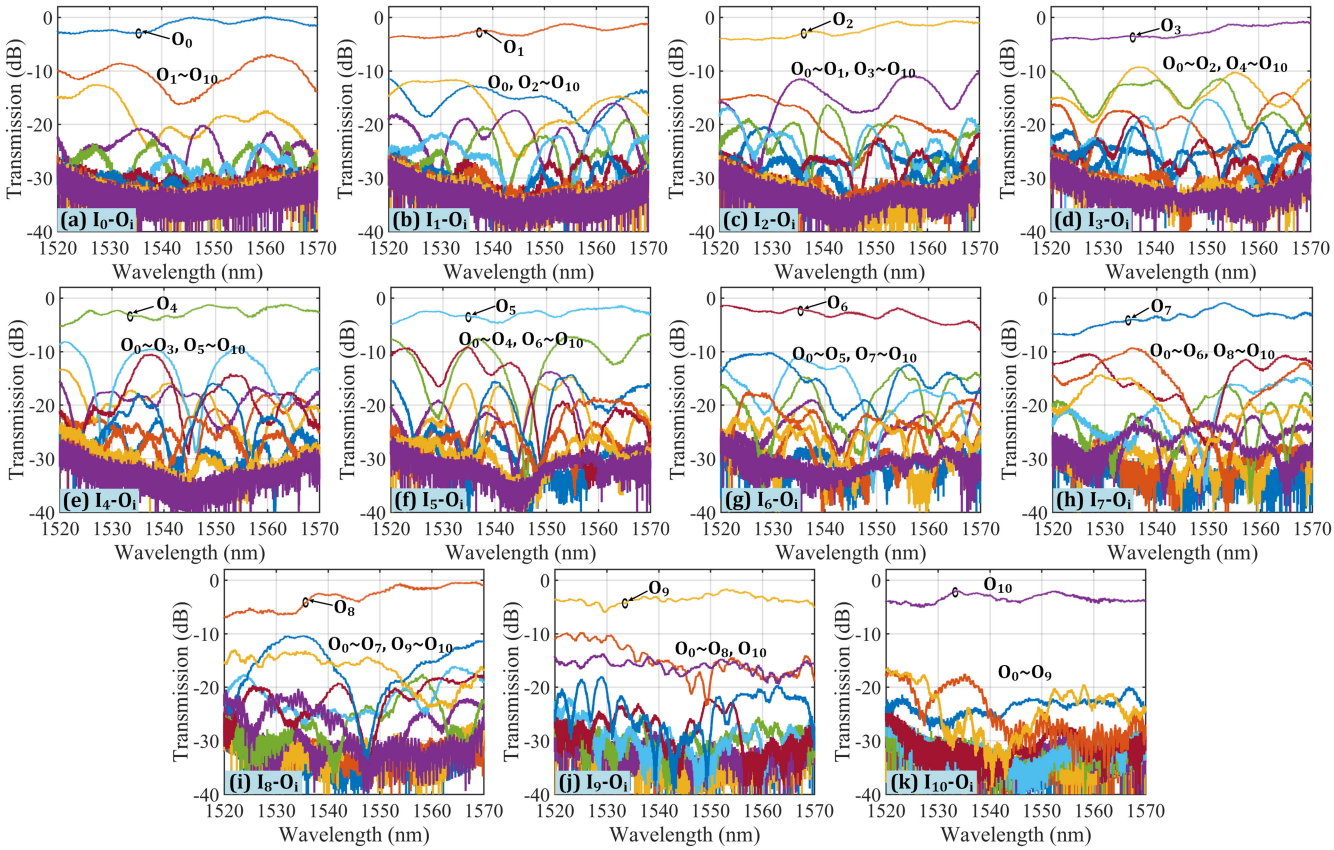

Fig. 6. The widths of the access and the bus waveguides vary by −20 nm. (a)–(k) illustrate the measured transmission responses at the 11 output ports of the mode demultiplexer (denoted as O_i, $i = 0 \sim 10$), when the light is injected from different input ports I_0–I_{10}, respectively.

III. Device Fabrication and Experimental Results

A. Fabrication Process

The SWG-based mode (de)multiplexers were fabricated on a SOI wafer with a 220-nm-thick silicon on top of a 3-μm silica buffer layer. The devices were firstly defined utilizing E-beam lithography (Vistec, EBPG-5200$^+$) and inductively coupled plasma (ICP, SPTS) etching, and then deposited with a 1-μm- thick SiO_2 cladding layer by plasma-enhanced chemical vapor deposition (PECVD, Oxford). A tunable continuous wave (CW) laser (Keysight 81960A) and an optical power meter (Keysight N7744A) were used to characterize the devices. The microscope photo of the fabricated 11-mode (de)multiplexer is shown in Fig. 3. The device consists of an 11-channel mode multiplexer (with input ports $I_0 \sim I_{10}$), a 70-μm-long multimode bus waveguide, and an 11-channel mode demultiplexer (with output ports $O_0 \sim O_{10}$). The footprint of this multiplexer is less than $507 \times 5.29\ \mu m^2$. Grating couplers were adopted for vertical coupling between the optical fibers and the silicon chip, with a coupling loss of ~7.0 dB/facet. When the signal is injected from the selected input port (I_i), high efficiency light is obtained from the corresponding output port (O_i). For instance, if a TE_0-mode signal is launched into the I_5 port, the light is coupled to the TE_5 mode of the bus waveguide by a SWG-based DC. After transmitting as the TE_5 mode in the multimode bus waveguide, the signal is subsequently demultiplexed by the mode demultiplexer and then outputs from the O_5 port. Scanning electron microscope (SEM, ZEISS) images of the asymmetric DCs and the SWG-based DCs used for different-order mode multiplexing are shown in Fig. 4.

TABLE II
Insertion Losses and Crosstalk Values of the Fabricated 11-Channel Mode (de)Multiplexer at 1545 nm

Input port	Mode order	Insertion loss (dB)	Crosstalk (dB)
I_0	TE_0	0.1	−17.4
I_1	TE_1	1.5	−17.1
I_2	TE_2	1.0	−15.4
I_3	TE_3	2.2	−16.7
I_4	TE_4	0.4	−17.0
I_5	TE_5	0.4	−23.7
I_6	TE_6	2.6	−20.8
I_7	TE_7	1.2	−22.1
I_8	TE_8	1.9	−26.1
I_9	TE_9	2.4	−26.4
I_{10}	TE_{10}	2.3	−19.8

B. Experimental Results

Measured transmission responses and modal crosstalk values at the 11 output ports of the fabricated mode (de)multiplexer are shown in Fig. 5. The transmission spectra of the mode (de)multiplexer were normalized to that of the identical grating couplers fabricated on the same wafer. Measured insertion

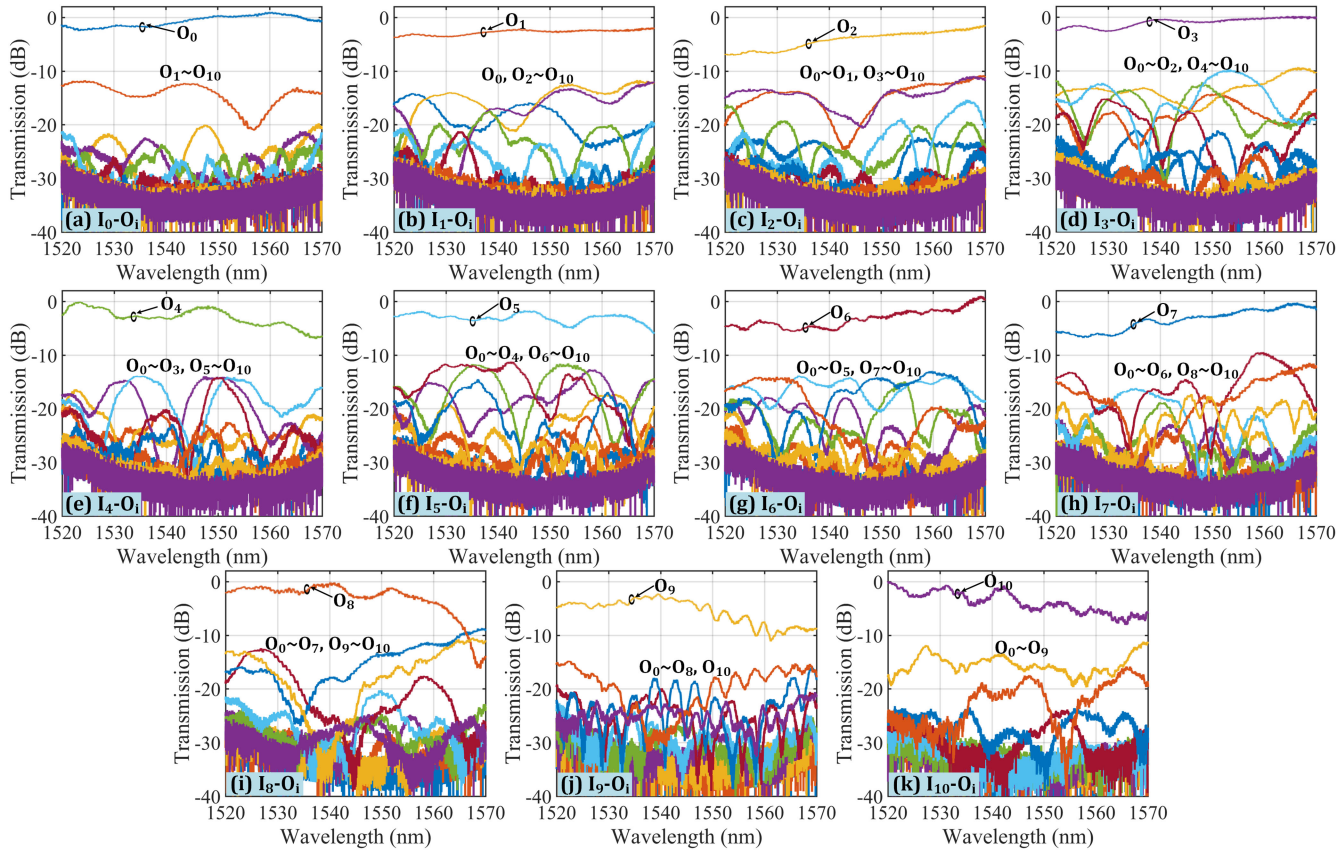

Fig. 7. The widths of the access and the bus waveguides vary by +20 nm. (a)–(k) illustrate the measured transmission responses at the 11 output ports of the mode demultiplexer (denoted as Oi, i = 0 ∼ 10), when the light is injected from different input ports I_0–I_{10}, respectively.

losses ranging from 0.1 dB ∼ 2.6 dB, and the crosstalk values ranging from −15.4 dB to −26.4 dB are obtained at 1545 nm, for all the 11 channels. In the wavelength range of 1520 nm to 1570 nm, the overall insertion losses are lower than 5.2 dB, and the crosstalk values are below −10.0 dB. More experimental results are detailed in Table II.

For comparison, simulated transmission spectra are also presented, as shown by the black dashed curves in Fig. 5(a–k). It can be seen that the experimental results agree with the simulations. The relatively high insertion losses can be mainly attributed to the imperfect mode coupling condition caused by the fabrication process, which can be further reduced by improving the fabrication accuracy. In addition, one can also optimize some DCs' coupling lengths and shift the central operation ranges to 1545 nm, which may be helpful to improve the devices' performances at the band edges.

C. Characterization of the Device Tolerance

To estimate the influence caused by δ variation, we simulated the performance of the DCs for TE_9 mode, the worst channel according to the experimental results. When the δ value varies by ±3% (equivalent to ±9 nm), which is sufficient to mimic the waveguide width fluctuation caused by the fabrication process [35], the insertion losses change by less than 0.5 dB at 1545 nm.

Furthermore, we investigated the device tolerance to waveguide width variations by fabricating various mode (de)multiplexers with different waveguide widths on the same wafer. We varied the widths of the access and the bus waveguides by ±20 nm, and provide the measured transmission responses as shown in Fig. 6 and Fig. 7, respectively. If the widths of the access and the bus waveguides vary by ±20 nm, the device can still operate with acceptable insertion losses and crosstalk values. The overall insertion losses remain lower than 4.0 dB, and the crosstalk values are still below −10.4 dB at1545 nm for all the 11 channels. In the whole C-band, the insertion losses are lower than 6.1 dB, and the crosstalk values are below −7.3 dB. The performance of device can be further improved by optimizing the structural parameters. Achieving low crosstalk values becomes the main challenge for realizing high-tolerance mode (de)multiplexers, and new schemes for suppressing the crosstalk need to be explored.

IV. Conclusion

We have proposed and experimentally demonstrated a silicon 11-mode (de)multiplexer on single polarization by introducing SWG-based DCs, which supports TE_0 ∼ TE_{10} modes. It achieves the highest-order mode (de)multiplexing on a silicon chip. For all the 11 channels, low crosstalk values (−15.4 dB ∼ −26.4 dB) and low insertion losses (0.1 dB ∼ 2.6 dB) at 1545 nm are obtained. Owing to the flexible engineering of the effective refractive index in the SWG structure, the demonstrated mode (de)multiplexers are tolerant to waveguide width

variations. If the waveguide widths vary by ± 20 nm, the mode (de)multiplexer shows an insertion loss lower than 4.0 dB and a crosstalk value below -10.4 dB at 1545 nm. These results can be further optimized by modifying structural parameters. The proposed device has the potential to achieve even higher-order mode multiplexing or combine with polarization division multiplexing (PDM) scheme to further scale the transmission capacity.

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